64Mb COTS DRAMs: A Variety of SEE Responses

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Advanced commercial DRAMs are particularly attractive to designers for space applications needing large memory arrays due to resulting savings in mass, volume, and power. The variety of manufacturers producing DRAMs makes it likely that of at least one can be found having suitable fortuitous radiation resistance. This paper will summarize the test methodology developed and the test results obtained so far – part way through an ambitious survey of single-event responses of current 64Mb choices. In addition to measurements of latchup (if any) and cell upset cross sections, single-ion-induced functionality interrupts, stucks, and soft error clusters have been observed.

* Work performed by the Jet Propulsion Laboratory, California Institute of Technology under contract with the National Aeronautics and Space Administration with support from NASA Code AE.

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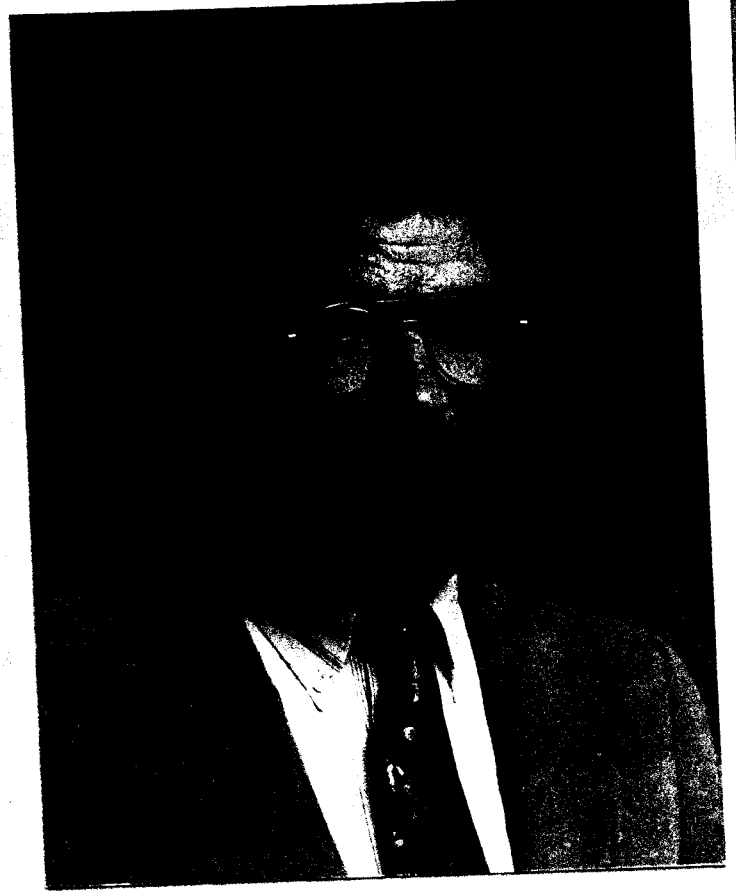

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ABSTRACT

Advanced commercial DRAMs are particularly attractive to designers for space applications needing large memory arrays due to resulting savings in mass, volume, and power. The variety of manufacturers producing DRAMs makes it likely that of at least one can be found having suitable fortuitous radiation resistance. This paper will summarize the test methodology developed and the test results obtained so far – part way through an ambitious survey of single-event responses of current 64Mb choices for the X-2000 project. In addition to measurements of latchup (if any) and cell upset cross sections, single-ion-induced functionality interrupts, stucks, and soft error clusters have been observed.

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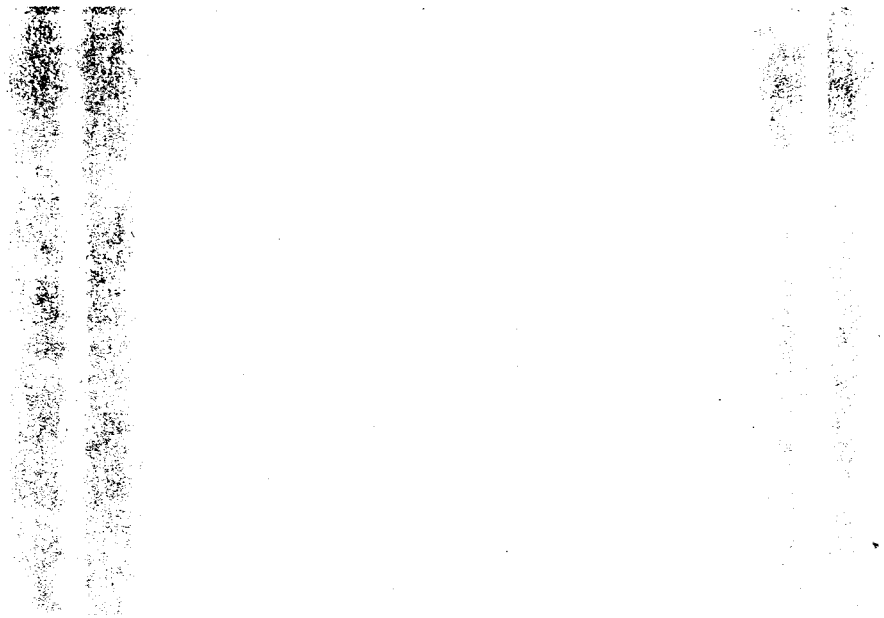
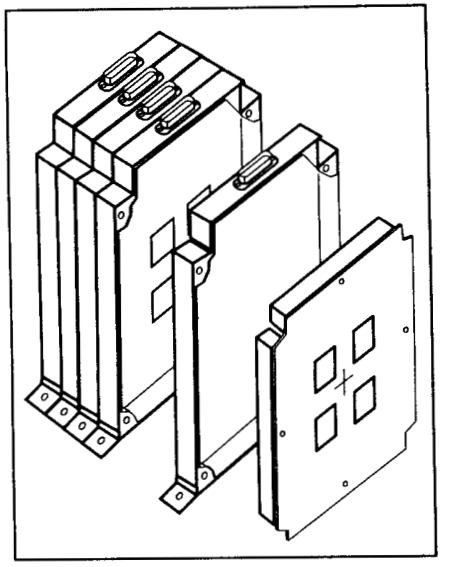


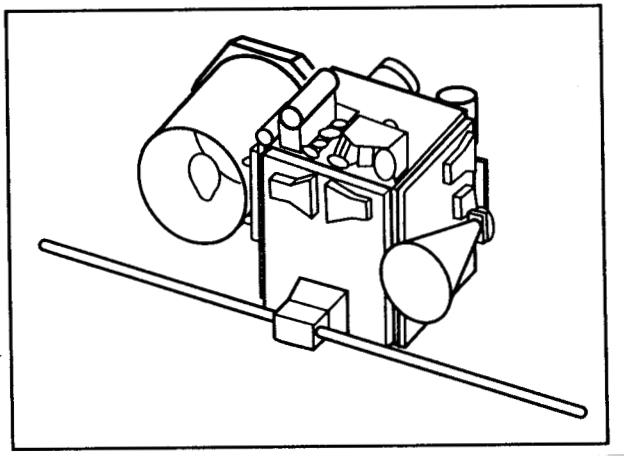
The PROJECT

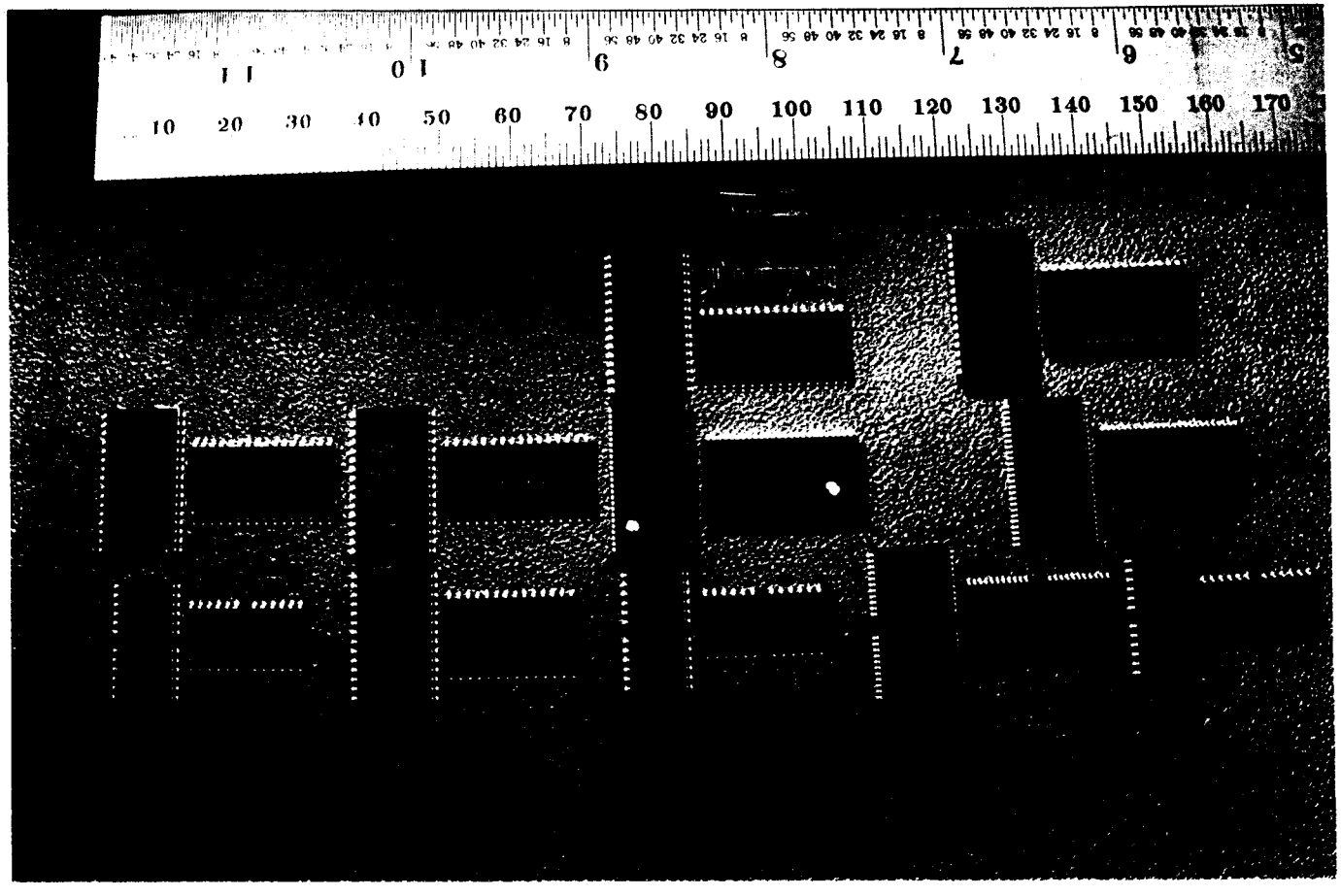
The X-2000 project is developing an innovative modular design for spacecraft avionics intended to serve as the basis for several spacecraft targeted for a variety of interesting destinations: Europa (Is there life under the ice of this moon of Saturn?), a close encounter with the sun, and Pluto, the only planet we haven't yet visited robotically. The present concept consists of configurable stacks of MCMs (multi-chip modules) with about 6 cm x 6 cm of circuitry surrounded by elastomer interconnects. This design requires high density, low power memory "slices" of half gigabyte capacity or larger (including error connection). Some of the missions, Europa particularly, will require operation in very high radiation environment. Identifying suitable COTS devices is very important if X-2000's missions are to succeed.



The PLAN

The X-2000 Europa mission is particularly severe from a radiation standpoint in that several megarads(Si) of ionizing dose (mostly from electrons) is expected behind 100 mils of Al shielding! The survey of COTS DRAMs starts with (1) heavy ion latchup testing. As a secondary result of this testing other single event effects data are captured. The goal is to identify as many manufacturers that don't suffer from destructive single event effects as possible for the next step, (2) total dose characterization. Finally, the two manufacturers with the highest dose performance will be (3) single event tested thoroughly with both heavy ions and protons. Currently, we are almost done with step #1.



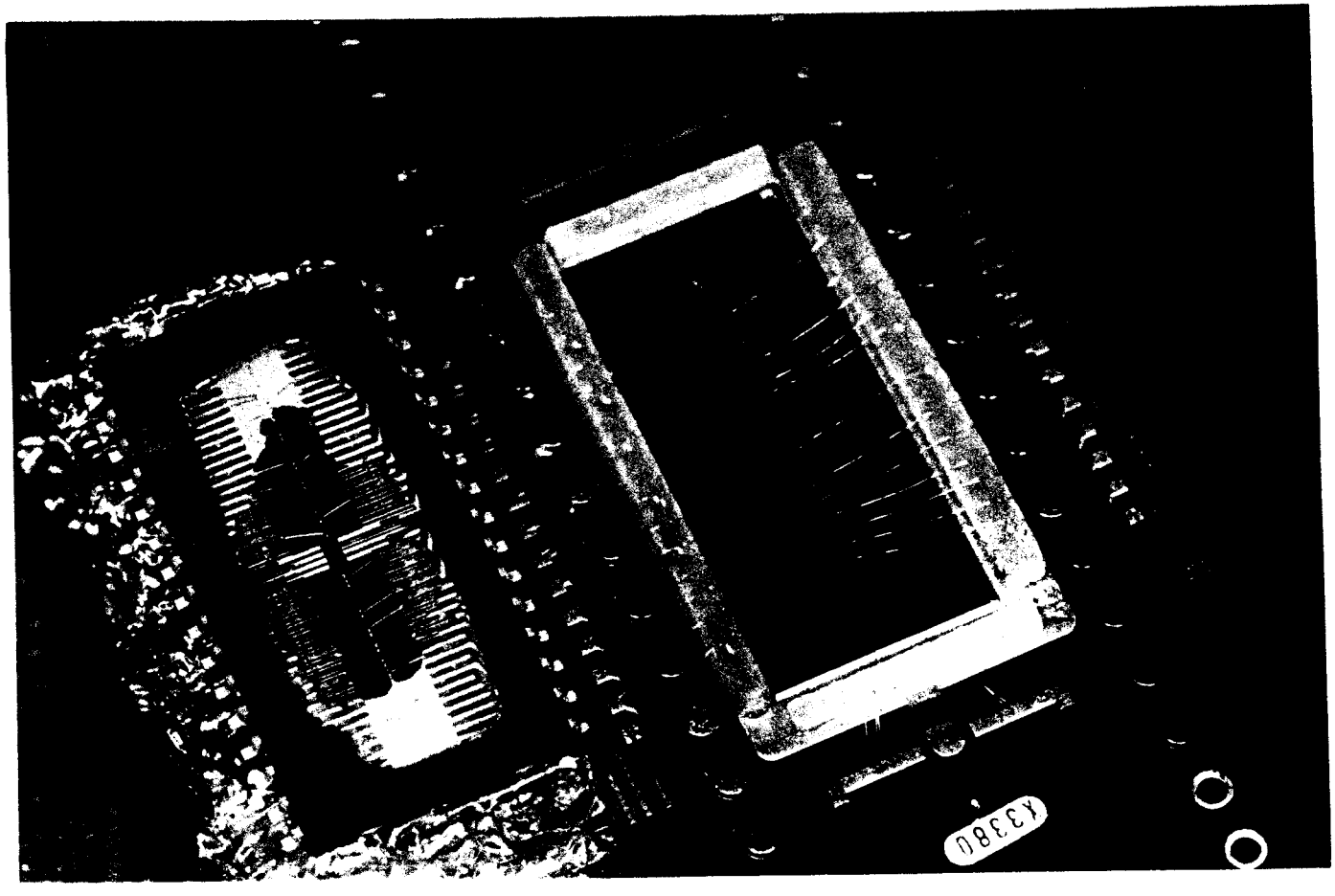


The TEST CANDIDATES

The photo show two samples of each device type which have been tested or will be soon. The bottom row shows 16Mb DRAMs tested as a scaling comparison and fallback if no "good" 64Mb candidates emerged. From left to right, the manufacturers are Toshiba, Samsung, Hitachi, OKI and Fujitsu. The next row is the 64Mb devices from Toshiba, Samsung, Hitachi, and NEC. Above the NEC 64Mb devices are Micron 64Mb devices, while above the Hitachi 64Mb DRAMs are Hitachi 128Mb devices (to be tested next month; bare dice are also shown.)

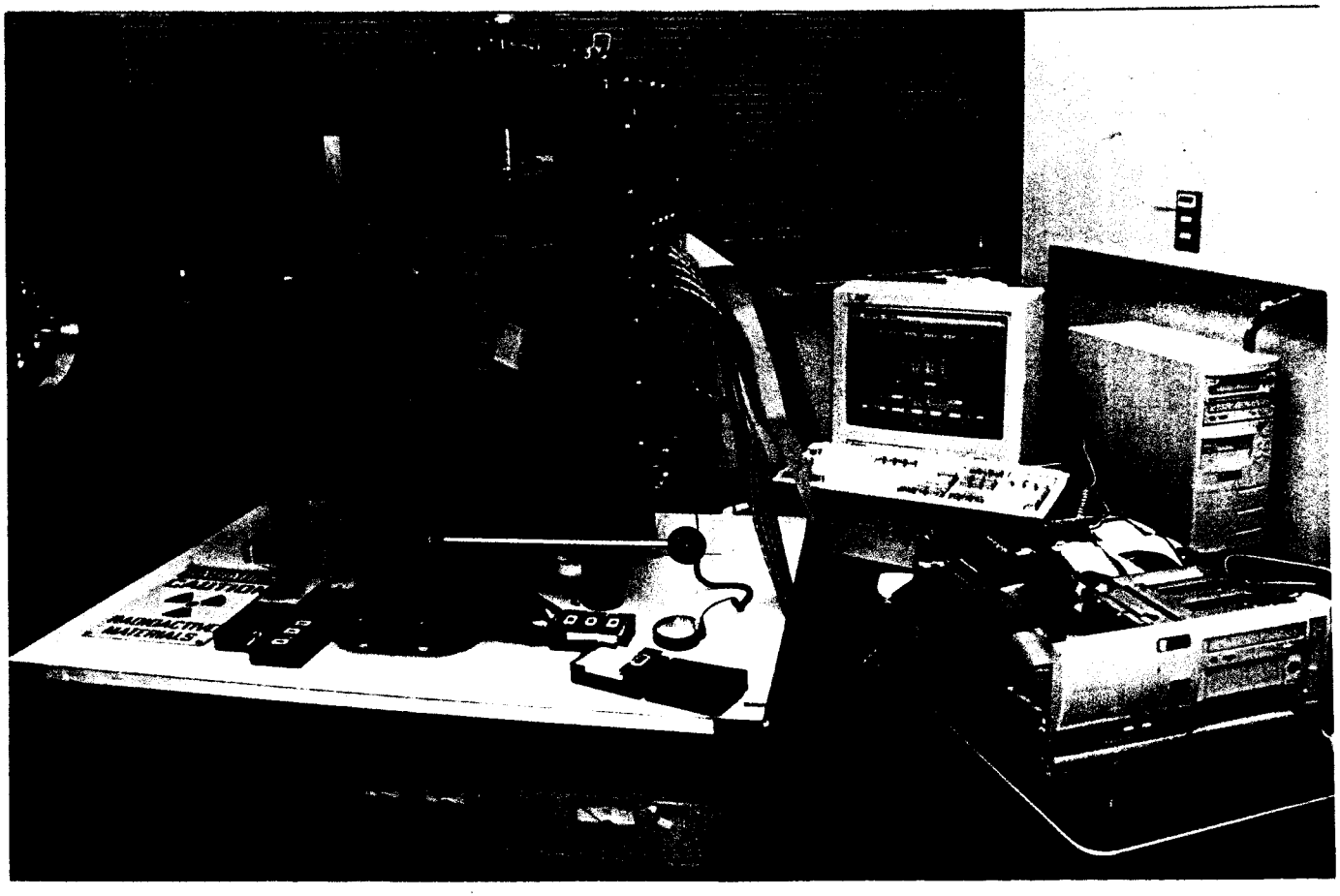
DEVICE PREPARATION

Preparing the devices for heavy ion testing proved to be a significant challenge. This photo shows Technician Mike O'Connor using the jet acid etch apparatus to remove the plastic packaging surrounding the part. All of the devices tested use a lead frame to connect the bond wires to the pins. This also overlies the die and must be removed. Fortunately, all the lead frame insulators were removed with the same etching process. Subsequent to this step, the die will be rebonded to a custom chip carrier board.



DEVICE PREPARATION

A partially etched Toshiba 64Mb device and the final testable chip-on-carrier- board are shown in this photo. Note that, on the partially etched device, there is a central region where the die is exposed, then a concentric region where the white colored lead frame insulator remains and finally a concentric region where the black package plastic is still intact. Underneath the rebonded device, the carrier boards have pins that accommodate a standard 40-pin DIP socket.



The TEST APPARATUS

A new software-driven test setup was developed for the COTS DRAM survey and is shown fully set up for testing in JPL's Californium-252 vacuum chamber. A custom PCI bus interface board initiates the signals to and receives data from the DUT (device under test). Forty pin ribbon cables carry the signals through the vacuum bulkhead. Small custom buffer boards with differential line drivers and receivers ensure signal integrity. The custom DUT card supports testing any one of three devices without breaking vacuum to change parts. Finally, a quad power supply, controlled by a second PC, provides power for the three devices and the DUT card itself. This PC monitors and records DUT current and detects and counts latchups.

TEST RESULTS

LATCHUP

Surprisingly most of the devices did not exhibit latchup when irradiated with more than 10^6 ions of 360 MeV gold ions with a incident LET of 80 MeV per mg/cm^2 and a range of almost 30 μm. Two exceptions are the Micron 64 Mb DRAM which latched readily ($\sigma > 10$ cm^2) and the Toshiba 64Mb DRAM which exhibited a small cross section at LETs above. The Toshiba latchup was so rare that we felt another lot might be latchup immune, and we have not eliminated it from subsequent radiation characterization (Micron was eliminated).

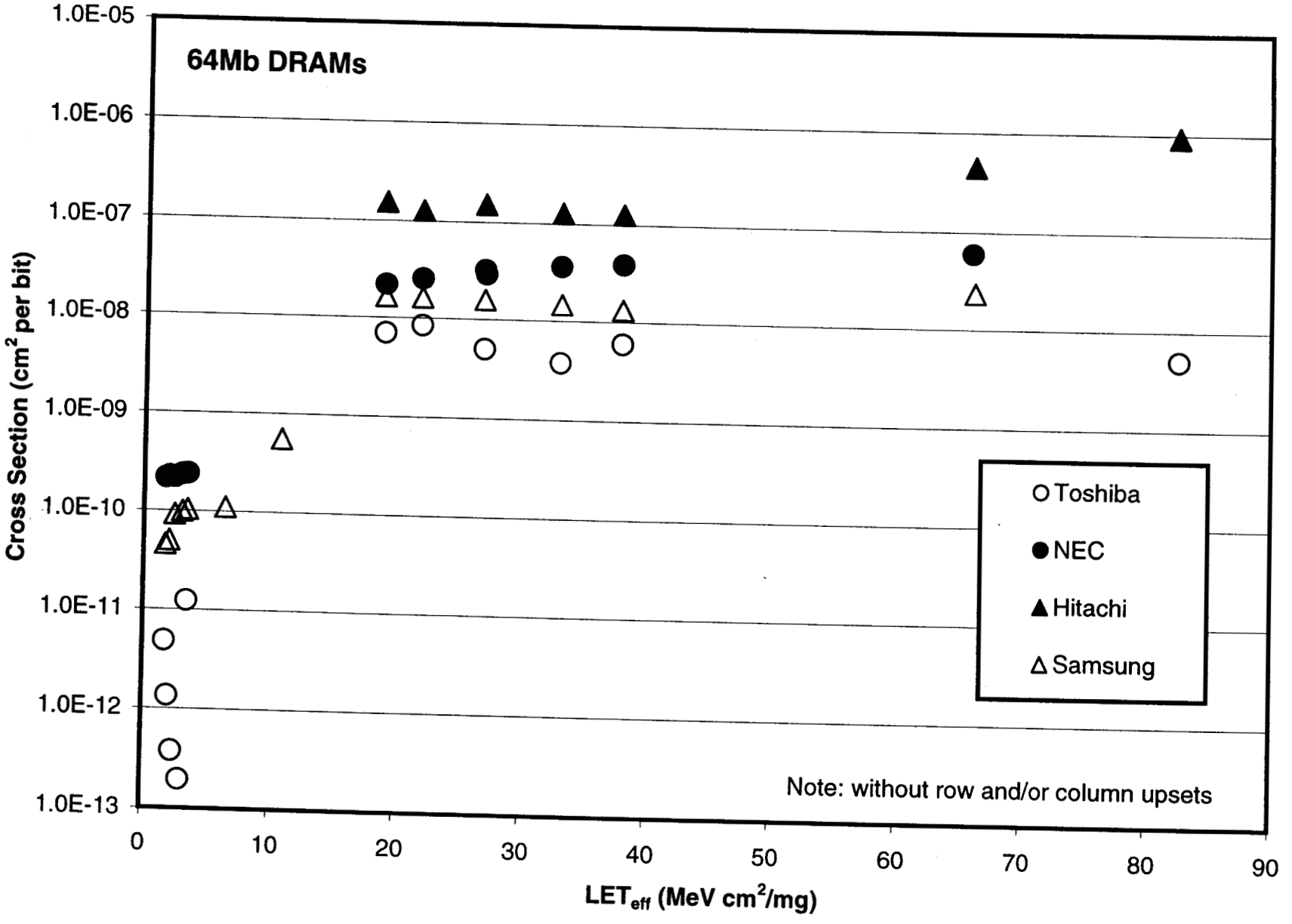
STUCKS

The DRAMs exhibited only a few micro-dosed bits, even under the heaviest irradiations. The Toshiba possibly had SEGR-type permanent damage under gold irradiation (LET=80) with a cross section of about10^{-2} cm^2; this result is not conclusive and is still under investigation.

FUNCTIONAL INTERRUPTS

All the devices exhibited SEFI (single event functional interrupt), but with different LET thresholds and cross sections. Detailed characterization of SEFI is deferred until the heavy ion testing of phase 3.

CELL UPSETS


64Mb DRAMs
Cross Section (cm² per bit)
1.0E-05
1.0E-06
1.0E-07
1.0E-08
1.0E-09
1.0E-10
1.0E-11
1.0E-12
1.0E-13
0
10
20
30
40
50
60
70
80
90
LET_eff (MeV cm²/mg)
Toshiba
NEC
Hitachi
Samsung
Note: without row and/or column upsets

UPSET CLUSTERS

Average Cluster Size
(multiple bit upsets cause values greater than 1)

	LET (MeV per mg/cm^2) 1.7	19	80
Toshiba	1.0	1.5	2.2
NEC	1.0	1.6	2.7
Hitachi	1.0	1.1	3.3
Samsung	1.0	1.7	3.1

CONCLUSIONS

Since single event latchup is a problem for only a few types of advanced DRAMs, the "success" of the manufacturer survey now depends on the results of the follow-on total dose testing. However, there are so many choices (with more coming) that the survey is likely to identify some types that are significantly better.